REMARKS/ARGUMENTS

<u>35 USC §103(a)</u>
Applicant thanks the Examiner for the detailed comments and remarks contained in the instant Office Action. Applicant respectfully requests the Examiner's further consideration of the following remarks.

In the instant Office Action, claim 1 is rejected under §103(a) over the newly cited combination of Shu (US 5,594,839) and Hirahara (US 4,910,603). This rejection is respectfully traversed.

Claim 1 requires, *inter alia*, that a full line of dither values be read and output into the buffer memory. Claim 1 further requires that a full line of dither values in the buffer be output therefrom.

In rejecting claim 1, the Examiner asserts that Hirahara discloses the above two limitations. For reasons as follows, it is respectfully submitted thatHirahara does not in fact disclose the above two limitations.

Hirahara describes a multi-level dither matrix ROM 22 that stores various control levels representing the amount of energy to be supplied to individual heating elements of a print head *(see col. 7, lines 57 - 61)*. The description of Hirahara at col. 6, line 61, - col. 7, line 45 describes how the multi-level dither matrix ROM 22 is used.

According to this description of Hirahara, 8 bit gradation data is stored in one of two buffers RAM1RD and RAM2RD. Data is read from RAM1RD and RAM2RD and supplied to the multi-level dither matrix ROM 22. The data read from RAM1RD/RAM2RD and supplied to the multi-level dither matrix ROM 22 appears to represent address data identifying a coordinate within the multi-level dither matrix ROM 22 *(see for example the description at col. 7, lines 20 - 34)*. Based on this address data, the multi-level dither matrix ROM 22 outputs a 6-bit control level representing an amount of energy to be supplied to individual heating elements of a print head.

With reference particularly to the description of Hirahara at col. 7, lines 30 - 34, it is described that when given as an address an input level of "7" for the dot at $x = 1$ and $y = 2$, a control level of "8" is outputted. Applicant respectfully points out that neither the input nor the output to/from multi-level dither matrix ROM 22 is a full line of dither values. On the contrary, the multi-level dither matrix ROM 22 appears to output data on a dot-by-dot basis.

Moreover, the inputs and outputs to/from the multi-level dither matrix ROM 22 do not appear to be dither values. The input into the multi-level dither matrix ROM 22 is explicitly described as a combination of an input level, an x-coordinate, and a y-coordinately. Similarly, the output from the multi-level dither matrix ROM 22 is explicitly described as a control level representing an amount of energy to be supplied to individual heating elements of a print head.

It is further noted that Hirahara does not even describe outputting data <u>into</u> the multi-level dither matrix ROM 22. It appears that the multi-level dither matrix ROM 22 is already filled with information. Data is not output into the multi-level dither matrix ROM 22 to fill it up.

For reasons as presented above, Applicant respectfully submits that the combination of Shu and Hirahara fail to prejudice the novelty and inventiveness of claim 1. The deficiencies of Shu as recognized by the Examiner are not made up for by Hirahara. Specifically, not even the combination of Shu and Hirahara teach or suggest:

1)   Outputting a full line of dither values in to a buffer memory; and
2)   Outputting a full line of dither values from the buffer memory.

Hirahara only outputs a 6 bit control level, which firstly represents only the data of one dot, and secondly, is not a dither value.
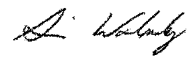
Claims 2 to 6, which are dependent from claim 1, are submitted to be novel and inventive at least by virtue of their dependency from claim 1.

The Examiner's reconsideration of the application in light of the above remarks is respectfully sought. Applicant looks forward to word of further official communication in due course.

Very respectfully,

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